WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a semiconductor substrate;

an N-channel MISFET and a P-channel MISFET provided on the semiconductor substrate, each of the N- and P-channel MISFETs being isolated by an isolation region and having a gate insulating film;

a first gate electrode film provided on the gate insulating film of the N-channel MISFET and composed of a first metal silicide;

a second gate electrode film provided on the gate insulating film of the P-channel MISFET and composed of a second metal silicide made of a second metal material different from a first metal material composing the first metal silicide; and

a work function of the first gate electrode film being lower than that of the second gate electrode film.

2. The semiconductor device according to claim 1, wherein the second gate electrode film includes at least one material selected from the first metal material and a third metal silicide, the third metal silicide having the same constituent material of the first metal silicide and lower silicon content than the first metal silicide.

3. The semiconductor device according to claim 2, wherein said one material selected from the first metal

material and the third metal silicide being present at an interface being in contact with at least the gate insulating film.

4. The semiconductor device according to claim 2, wherein said one material selected from the first metal material and the third metal silicide is a precipitation layer.

5. The semiconductor device according to claim 2, wherein said one material selected from the first metal material and the third metal silicide is present in a form of a particle.

6. The semiconductor device according to claim 1, wherein the number of silicon atoms per unit volume is 2.5 times more than the number of metal atoms per unit volume in a composition ratio between silicon and metal composing the first metal silicide.

7. The semiconductor device according to claim 2, wherein the number of silicon atoms per unit volume is not more than the number of metal atoms per unit volume in the composition ratio between silicon and metal composing the third metal silicide.

8. The semiconductor device according to claim 1, wherein the first metal silicide is tungsten silicide.

9. The semiconductor device according to claim 1, wherein the second metal silicide is composed of at least one kind of metal silicide selected from the metal silicides of platinum, palladium, and rhodium.

10. The semiconductor device according to claim 1, wherein one material selected from the metal film and the metal silicide film is provided on source and drain regions of the N-channel MISFET and the P-channel MISFET.

11. The semiconductor device according to claim 10, wherein said one material selected from the metal film and the metal silicide film provided on the source and drain regions of the N-channel MISFET is composed of one material selected from at last one kind of metal film and metal silicide film selected from titanium, zirconium, hafnium, tantalum, and niobium.

12. The semiconductor device according to claim 10, wherein said one material selected from the metal film and the metal silicide film provided on the source and drain regions of the P-channel MISFET is composed of one material selected from at last one kind of metal film and metal silicide film selected from platinum, palladium, and rhodium.

13. The semiconductor device according to claim 10, wherein a semiconductor film is provided on extension regions of the N-channel MISFET and the P-channel MISFET as elevated source/drain regions.

14. A method of manufacturing a semiconductor device, comprising:

forming an isolation region in a semiconductor substrate to provide an N- and a P-channel MISFET

regions each surrounded by the isolation region;

forming an insulating film on the semiconductor substrate;

forming a conductive film on the insulating film;

patterning selectively the conductive film to provide a gate region in each of the MISFET regions;

forming source and drain regions in each of the MISFET regions for the patterned conductive film by a self-alignment way;

forming a sidewall insulating film around the patterned conductive film;

removing the conductive film and the insulating film of the gate region to provide a space region surrounded by the sidewall insulating film;

forming a gate insulating film on the N- and P-channel MISFET regions each surrounded by the space region, respectively;

forming a first metal silicide film on the gate insulating film within the space region to provide a first gate electrode film;

forming a metal film different from metal composing the first metal silicide film on the P-channel MISFET region; and

heat-treating the semiconductor substrate to form a second gate electrode film formed by a solid phase reaction between the first metal silicide film and the metal film, the second gate electrode film being

composed of a second metal silicide made of a second metal material different from a first metal material composing the first metal silicide.

15. The method according to claim 14, wherein the second gate electrode film is formed by changing into a film including at least one material selected from the first metal material and a third metal silicide, the third metal silicide having the same constituent material of the first metal silicide and lower silicon content than the first metal silicide.

16. The method according to claim 14, wherein the number of silicon atoms per unit volume is 2.5 times more than the number of metal atoms per unit volume in a composition ratio between silicon and metal composing the first metal silicide.

17. The method according to claim 14, wherein the number of silicon atoms per unit volume is not more than the number of metal atoms per unit volume in the composition ratio between silicon and metal composing the third metal silicide.

18. The method according to claim 14, wherein a tungsten silicide film is formed as the first metal silicide.

19. The method according to claim 14, wherein the second metal silicide is composed of at least one kind of metal silicide selected from the metal silicides of platinum, palladium, and rhodium.

20. The method according to claim 14, wherein one material selected from the metal film and the metal silicide film is formed on the source and drain regions of the N- and P-channel MISFETs during a process for forming the sidewall insulating film and the space region.

21. The method according to claim 14, wherein a process for forming one material selected from the metal film and the metal silicide film on the source and drain regions of the N- and P-channel MISFETs is carried out after the heat treatment.